What is claimed is:

1. A multi-stage amplifier comprising:

a first amplifier stage including at least one first transistor, said at least one first transistor selected to provide an optimum noise characteristic; and,

a second amplifier stage including at least one second transistor, said at least one second transistor selected to provide an optimum gain characteristic.

2. The multi-stage amplifier of claim 1, further comprising:

a third amplifier stage including at least one third transistor, said at least one third transistor selected to an optimum gain characteristic.

3. The multi-stage amplifier of claim 1, further comprising:

an input matching network coupled to an input of the first stage.

4. The multi-stage amplifier of claim 1, further comprising:

an output matching network coupled to an output of the second stage.

5. The multi-stage amplifier of claim 2, further comprising:

an output matching network coupled to an output of the third stage.

6. The multi-stage amplifier of claim 1, wherein the at least one first transistor comprises a number of transistors, the specific number selected to provide an optimum noise characteristic.

7. The multi-stage amplifier of claim 1, wherein optimum noise characteristic is provided by selecting an appropriate geometry for the at least one first transistor.

8. The multi-stage amplifier of claim 1, wherein optimum gain characteristic is provided by selecting an appropriate geometry for the at least one second transistor.

9. The multi-stage amplifier of claim 2, wherein optimum gain characteristic is provided by selecting an appropriate geometry for the at least one third transistor.

10. A method for producing a multi-stage amplifier, comprising the steps of:

selecting at least one first transistor for a first stage to provide an optimum noise characteristic; and,

selecting at least one second transistor for a second stage to provide an optimum gain characteristic.

11. The method of claim 10, comprising the further step of:

selecting at least one third transistor for a third stage to provide an optimum gain characteristic.

12. The method of claim 10, wherein the step of selecting at least one first transistor for the first stage to provide an optimum noise characteristic comprises selecting an appropriate geometry for the at least one first transistor.

13. The method of claim 10, wherein the step of selecting at least one second transistor for the second stage to provide an optimum gain characteristic comprises selecting an appropriate geometry for the at least one second transistor.

14. The method of claim 11, wherein the step of selecting at least one third transistor for the third stage to provide an optimum gain characteristic comprises selecting an appropriate geometry for the at least one third transistor.

15. The method of claim 10, comprising the further step of:

selecting an output matching network, said output matching network being coupled to an output of the second stage.

16. The method of claim 11, comprising the further step of:

selecting an output matching network, said output matching network being coupled to an output of the third stage.

17. A method for producing a multi-stage amplifier, comprising the steps of:

selecting at least one first transistor such that at least one noise circle and at least one gain circle intersect at or near the center of a corresponding Smith Chart for the amplifier; and,

selecting at least one second transistor such that at least one noise circle and at least one gain circle intersect at or near the center of the corresponding Smith Chart.